REMARKS/ARGUMENTS

1. **Request for Continued Examination:**

The applicants respectfully request continued examination of the above-indicated application as per 37 CFR 1.114.

2. **Rejection of Claims 1-13 under 35 U.S.C. 103(a):**

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. US patent NO. 6,605,838, in view of Nitayama et al. US patent No. 6,236,079, for reasons of record that can be found on pages 2-6 in the Office action identified above, which is part of paper no./mail date 012005.

Response:

Claim 1 has been amended to clearly define that the STI separates the annular drain of the vertical transistor from any other annular drain of adjacent vertical transistors. According to the amended claim 1, a vertical transistor is disposed in a trench capacitor and has an annular source and an annular drain placed around the deep trench and circularly encompassing the deep trench for forming an annular channel to raise sufficient current. Furthermore, the vertical transistor is completely compassed by the STI so that the STI spaces the annular source and annular drain from other sources or drains of other transistors.

According to the Office action, the Examiner admits that Mandelman does not teach that a STI being positioned around the deep trench; a gate conductive layer is electrically connected to a first contact plug and an annular drain being electrically connected to a second contact plug; and an annular drain is positioned next to the STI and the annular drains of adjacent vertical transistors is isolated from each other by the STI. And the Examiner mentions Nitayama has taught those contents according to Figs. 4A and 4B.

According to Nitayama's application, Fig.4A and 4B are cross-sectional views along lines 4A-4A' and 4B-4B' of Fig.3, showing a semiconductor memory device formed with planar transistors and trench capacitors, wherein each of the planar

transistor includes a **gate electrode 136** being a portion of the word line 136, and the trench capacitor includes a first trench fill 120, a **second trench fill 124**, a buried plate electrode 116, and a storage node insulating film 122. (col. 4, lines 16 and 64). Therefore, referring to Fig.4A together with Fig.4B, Nitayama only shows forming a contact structure 112 on the second trench fill 124 but teach nothing about forming a contact structure on the gate electrode 136 in any figures or specification.

In addition, although the drain 134 seems to be spaced from other devices by the STI 108 in Fig.4B, it cannot be known whether the drain 134 is actually separated from other drains of adjacent transistors since no other transistors are illustrated in Fig.4B. However, one could clearly read that the drain 134 positioned under the bit line contact 106 is a common drain of two adjacent transistors according to Fig.4A which is the other side view of the semiconductor memory device shown in Fig.4B. Nevertheless, in the Nitayama's application, it also has the description "adjacent transfer transistors formed in a given active area have a common N-type drain region 134 (col.4, lines 59-60)". Accordingly, Nitayama et al. never teach that an STI separates the annular drain of the vertical transistor from other drains of adjacent transistors.

To sum up, Nitayama et al. fails to teach the limitations of the amended claim 1 of the present application as follows: (1) a contact structure positioned on the gate conductive layer of the vertical transistor; and (2) a STI compassing the vertical transistor and separating the annular drain of the vertical transistor from drains of other adjacent transistors. Since Mandelman either doesn't teach these limitations, the Applicants believe the combination of Mandelman and Nitayama's applications cannot obtain all limitations of the amended claim 1 of the present application.

In connection with the third criteria, MPEP 2143.03 goes on the state:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385,

165 USPQ 494, 496 (CCPA 1970).

Applicants respectfully assert that none of the three criteria are met to sustain a 35 U.S.C. 103(a) rejection against claim 1 when combining Nitayama with Mandelman's applications. Therefore, the amended claim 1 should be allowable. Reconsideration of the amended claim 1 is thereby requested.

Regarding claims 4 and 5, the Examiner points out that Mandelman et al. teach a buried strap (86). However, the structure (86) is actually a drain/source diffusion region, not a buried strap (col. 5, lines 10-20 of the specification of Mandelman et al.). The buried strap of present application is located on the inner surface of the sidewall of the deep trench (claim 5), and therefore the buried strap of the present application is different from the drain/source diffusion region disclosed in the specification of Mandelman et al. Reconsideration of claim 4 and amended claim 5 is hereby respectfully requested.

According to claim 9 of this application, the passivation layer (152) directly covers the surface of the transistor (166) and the substrate (110). However, Fig.4B of Nitayama et al. shows that the second isolation layer (152) is disposed on the word line (102) and the first isolation layer (148), without contacting the substrate or the transistor. Therefore, the second isolation layer (152) of Nitayama et al. is different from this application. In addition, the first isolation layer (148) of Nitayama et al. is positioned on the planar transistor without contacting the surface of the substrate (114), thus the position of the first isolation layer (148) of Nitayama et al. is also different from the position of the passivation layer (152) of the present application. Accordingly, Figs.4A-4B and the specification of Nitayama et al. are all silent about teaching a passivation layer covering both the surface of the substrate and the transistor, which if the content of claim 9 of the present application.

Claim 12 is amended to clear define the position of the annular spacer (150). The annular spacer (150) of the present application circularly encompasses the **entire** upper trench portion (120). Although the Examiner alleges that Nitayama et al. also

teach a spacer (140) in their memory device, but the structure (140) in Figs.4A or 4B is a conformal silicon nitride barrier layer with uniform thickness (col. 5, lines 1-4), which is formed by a deposition process. Therefore, those skilled in the art could understand the silicon nitride barrier (140) is not a so-called spacer. Accordingly, Nitayama et al. do not teach about an annular spacer compassing the entire upper trench potion. Sequentially, Nitayama et al. fail to disclose forming a contact plug on an annular spacer.

To sum up, the combination of the applications of Mandelman et al. and Nitayama et al. still does not teach all the limitations of claims 4, 5, 9, 12-13 of the present application. In another aspect, since claims 2-13 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowable. Reconsideration of claims 2-13 is hereby respectfully requested.

3. New claim introduction:

Claims 14-15 are added for further defining the relative position between the annular spacer, the STI, and the second contact plug. No new matter is introduced. Claim 14 mentions that the second contact plug is positioned on the STI and the annular spacer through different sides of the second contact plug at the same time, so that the vertical DRAM of the present application has an asymmetric structure at the join portion of the second contact plug (156), the STI (146), and the annular spacer (150), as shown in Fig.1. Claim 15 describes that the annular spacer is positioned on an outer surface of the entire upper trench portion. Referring to the figures or specifications of Nitayama et al. or Mandelman et al., they do not teach an asymmetric structure or an annular spacer. Therefore, allowance of claims 14-15 is politely requested.

Claim 16 is added for clearly describing the annular drain has an asymmetric structure. No new matter is introduced. According to claim 16, the annular drain has different widths since the portion of the annular drain contacting the second contact plug has a large width. Referring to the prior arts, neither Mandelman et al nor Nitayama et al. disclose a contact plug contacting the drain, and the drains of the prior

arts all have symmetric structures. Therefore, the combination of the above-mentioned prior arts cannot obtain claim 16. Adoption of the new claim 16 is hereby requested.

Claims 17-29 are introduced for defining the method of forming the vertical DRAM of the present application. No new matter is entered. Consideration is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)